Theme B: Energy Harvesting-Aware Computation Circuits

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Fei Xia (Theme B Coordinator, Newcastle)

Staff and students involved in Theme B:
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Southampton: Bashir Al-Hashimi, Jatin Mistry

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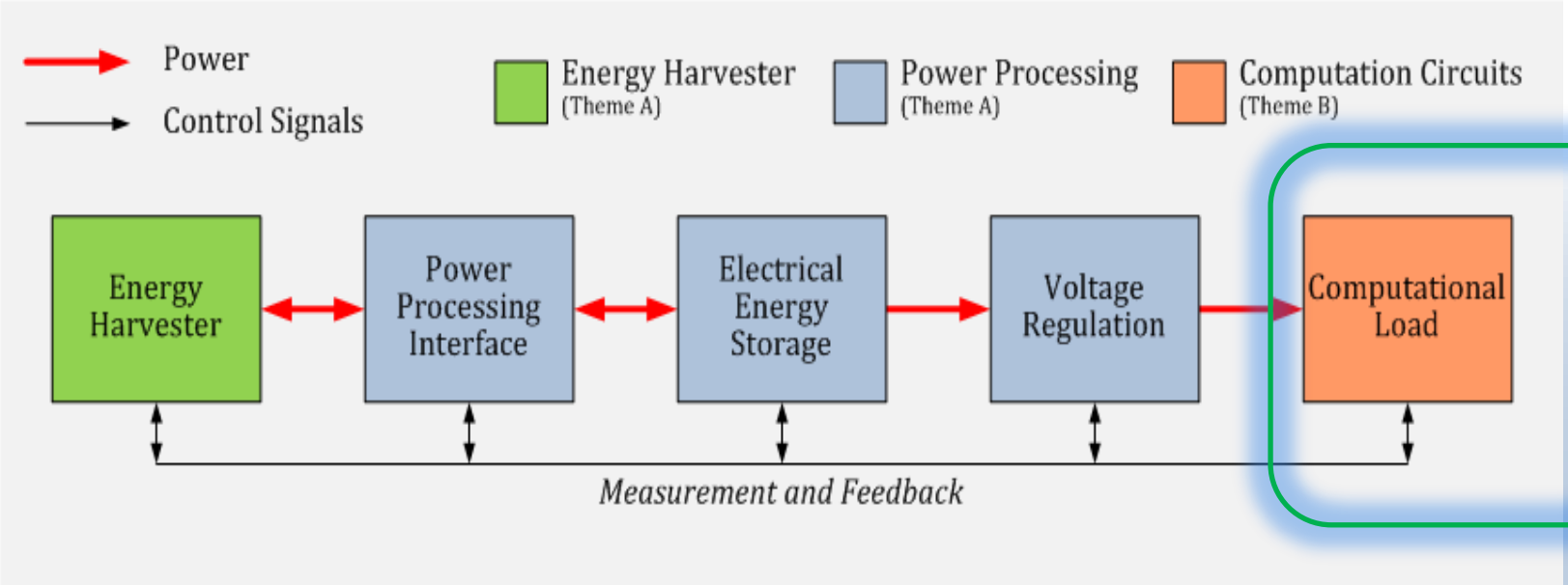
energy harvesting

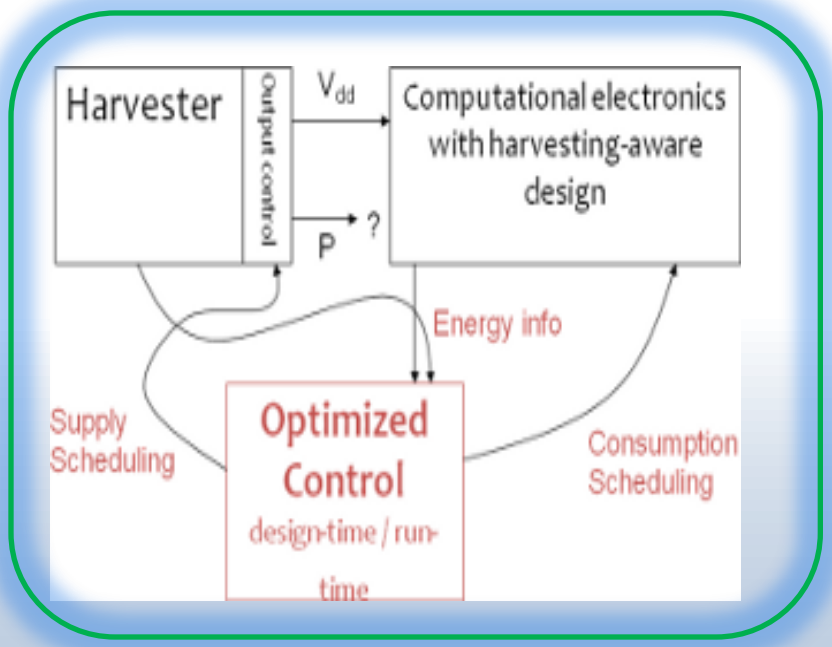
Theme B: Agenda

- Aims and objectives
- Key achievements
- Vision for the future



Vision, aims and objectives

- Energy harvester aware design methods for computational logic
- Capable of working under variable and unpredictable energy supply
- Circuit solutions for power control and management techniques
- Highly adaptive computational circuits



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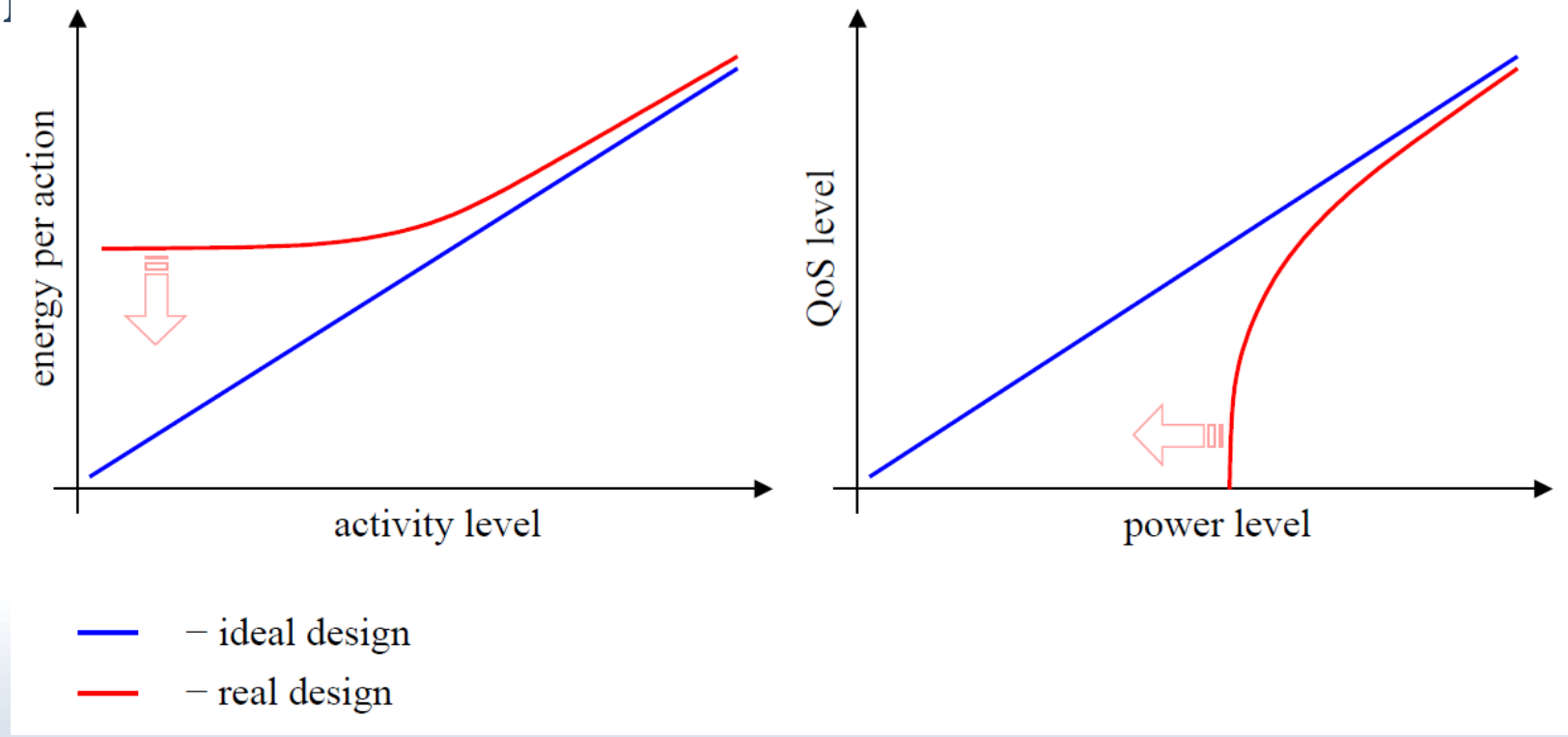
Key achievements

- Energy-modulated approaches
  - Power-adaptive and power-proportional system design
  - Self-timed logic for varying power conditions and near-threshold Vdd
  - Experiments with multiplier and FFT
  - System-level power management and optimization
  - Reference-free voltage sensing
  - Switched capacitor power delivery

Key achievements

- Infrastructure, processor, system construction and testing
  - Robust electronics for fluctuating power supply (Asynchronous SRAM and asynchronous FPGA)
  - Active power reduction in a microcontroller through sub-clock power gating
  - Chip design, testing system design, and testing results

Power-proportional computing



A. Yakovlev, Energy-Modulated Computing, Proc. DATE'11, Grenoble, March 2011, EDAA, pp. 1340-1345 (2011).

F. Xia, A. Mokhov, Y. Zhou, Y. Chen, I. Mitrani, D. Shang, D., Sokolov, A. Yakovlev, Towards power-elastic systems through concurrency management, IET Computers and Digital Technics, Vol.6, Iss. 1, pp.33-42, 2012.

Experiments with multiplier and FFT

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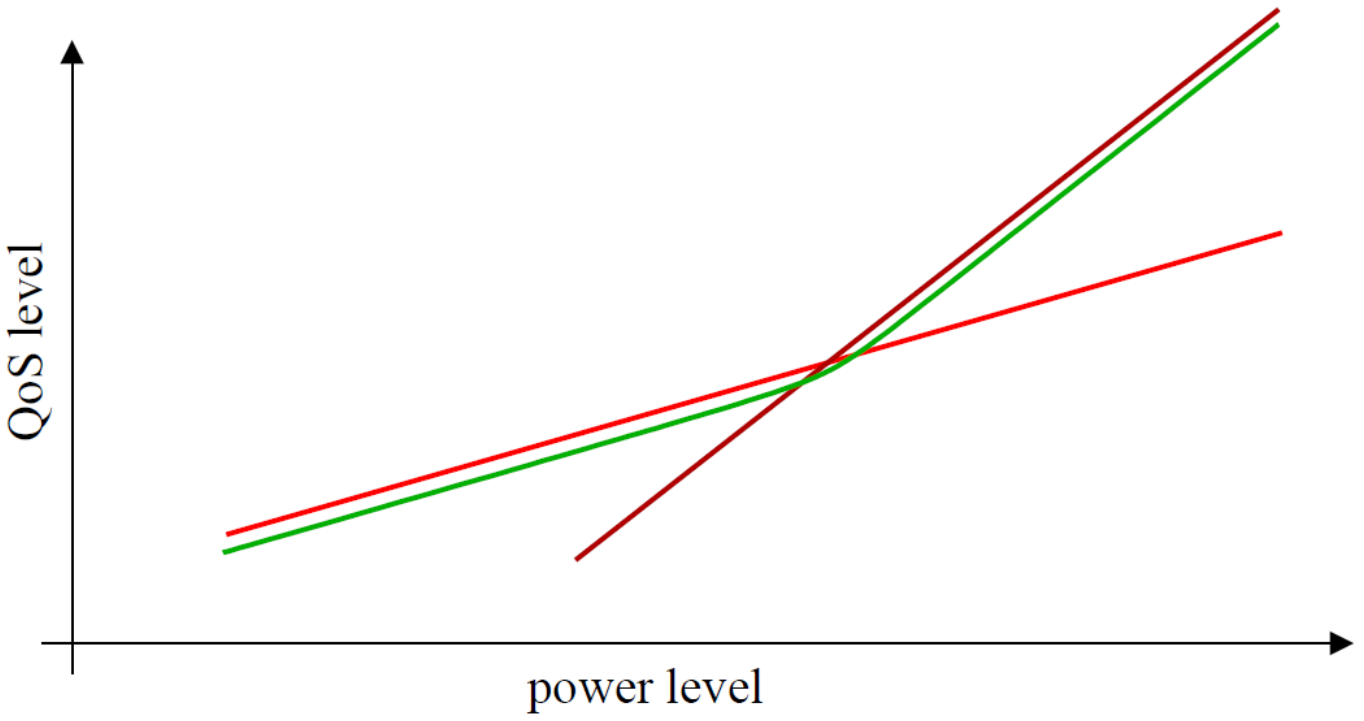


– power proportional design which is efficient for low power

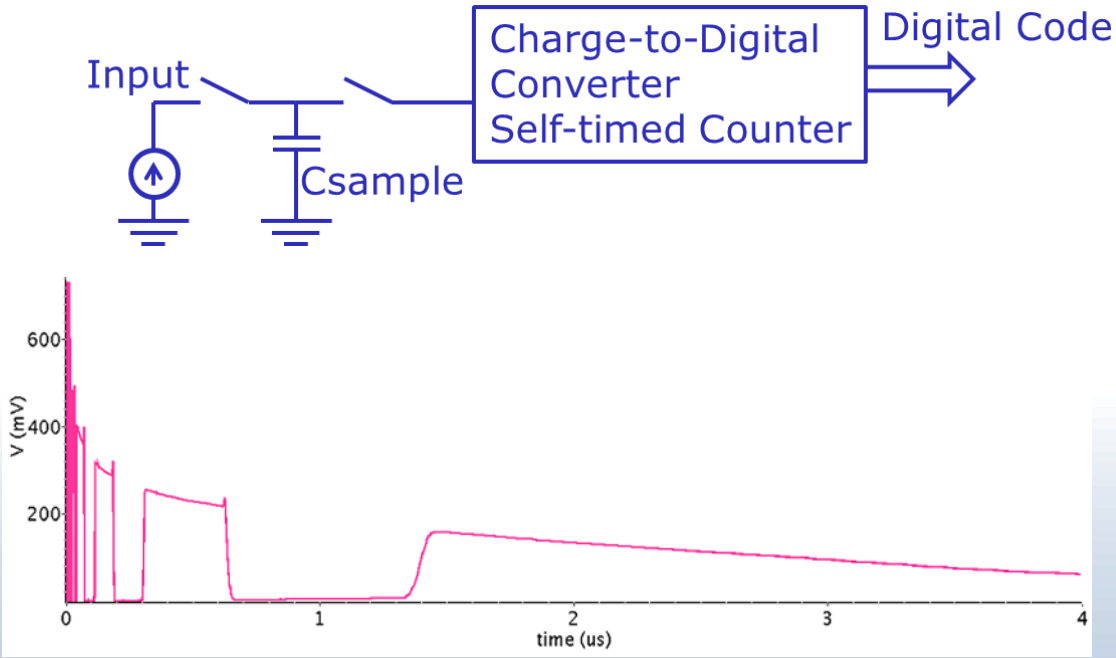
– less power proportionaldesign which is more efficient for high power

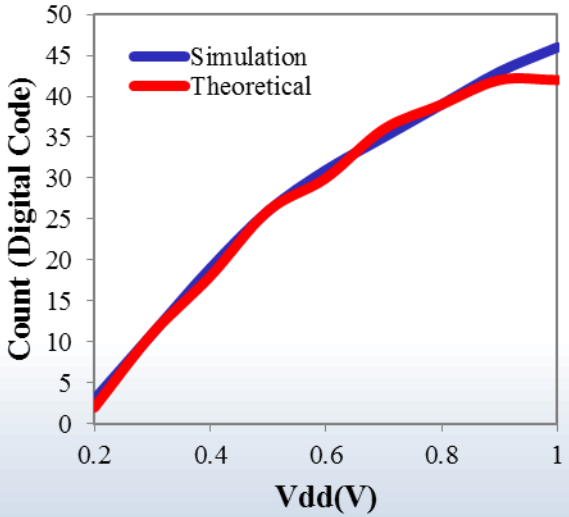
– hybrid design that can adapt to power levels

R. Ramezani, D. Sokolov, F. Xia, A. Yakovlev, Energy-modulated Quality of Service: New Scheduling approach, 11th IEEE FTFC, June 6-8, 2012, Paris.

Reference-free voltage sensing

- Voltage sensor requiring only timing reference

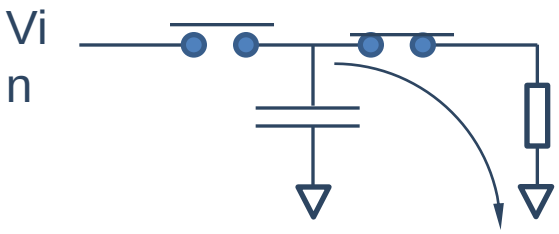




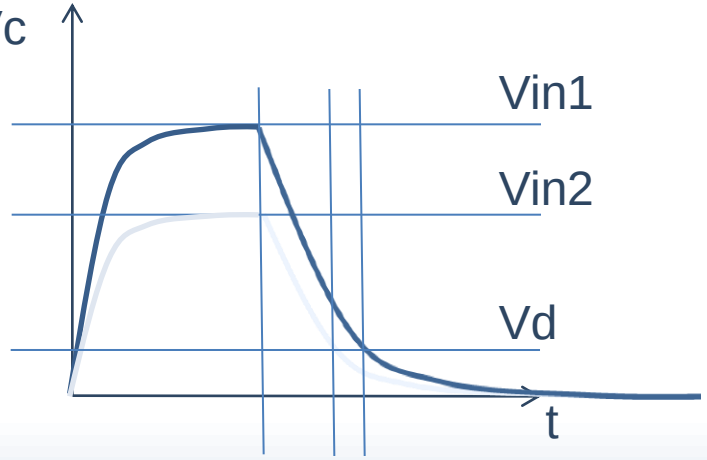
Apparatus and method for voltage sensing, Newcastle University, GB Patent Number 2479156, 30 March 2010.

Reference-free voltage sensing

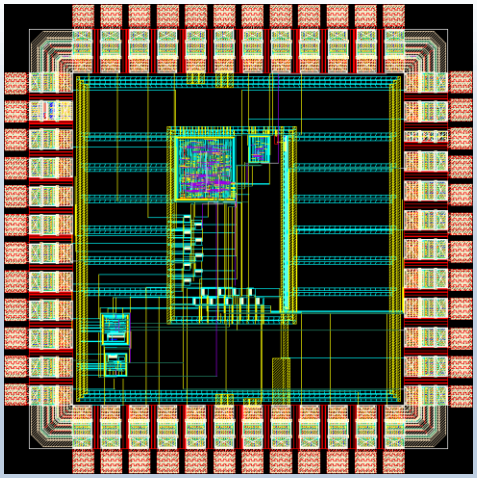
- Discharging until a certain Vd in order to get rid of timing reference



Discharging from Vc



Voltage sensor chip:
UMC CMOS 180nm



Vd is still a constant reference! *But it does not have to be externally sourced*. It could be based on some internal semiconductor characteristics

R. Ramezani, A. Yakovlev, F. Xia, J. Murphy D. Shang, "Voltage Sensing Using an Asynchronous Charge-to-Digital Converter for Energy-Autonomous Environments", IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), [in press].

Switched capacitor power delivery

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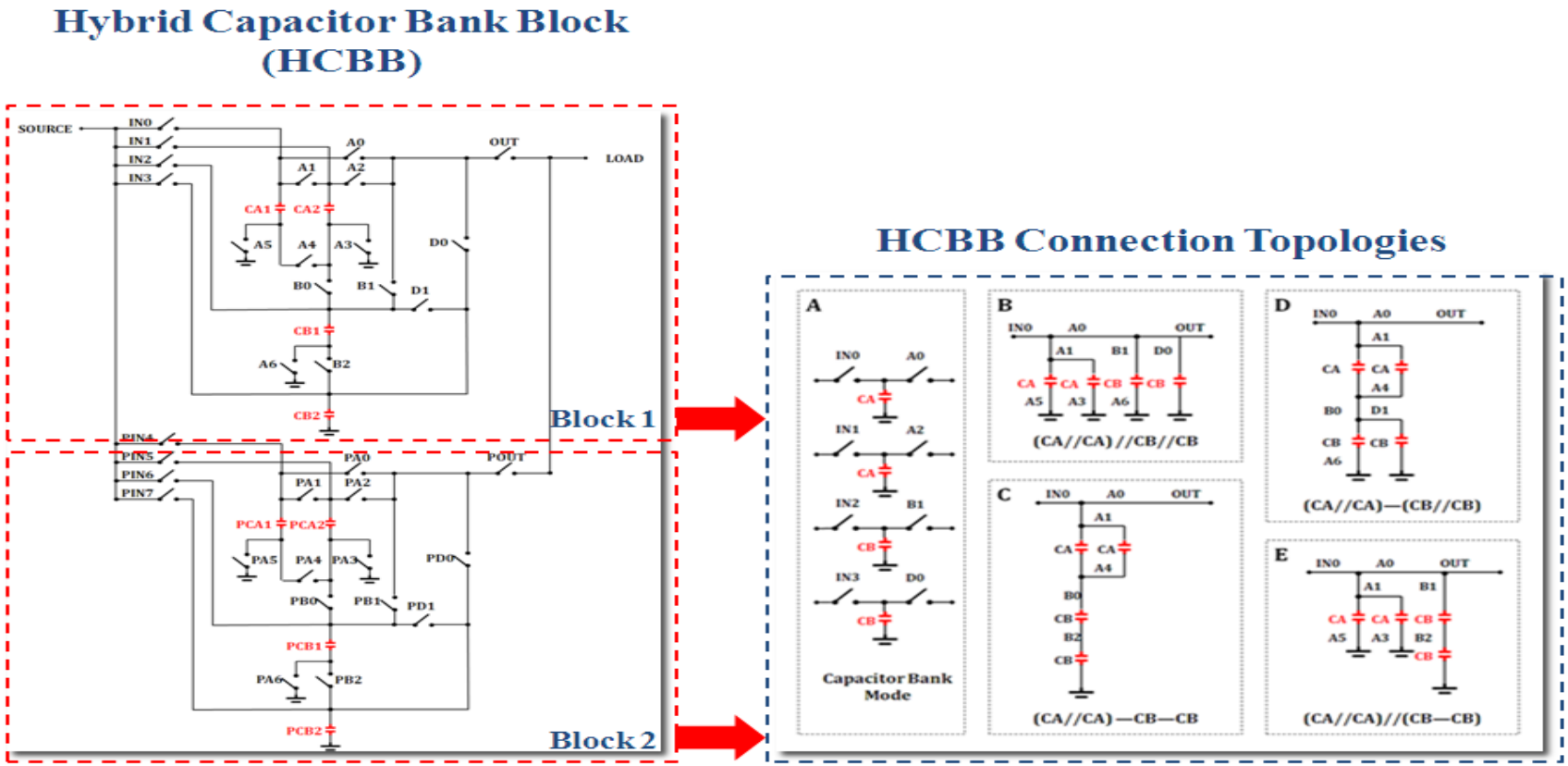
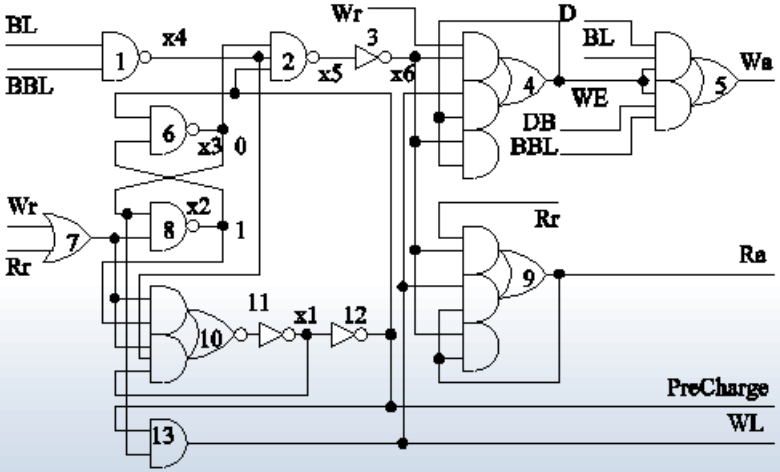
- HCBB design can be dynamically configured to work in CBB or Switched Capacitor Converter (SCC) mode

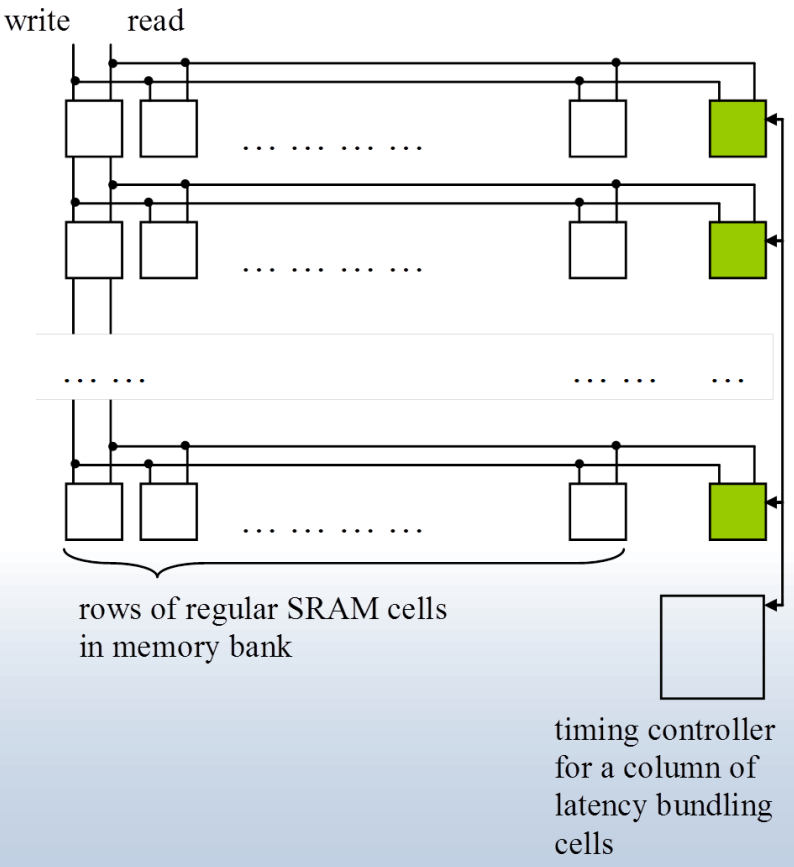


X. Zhang, D. Shang, F. Xia, A. Yakovlev, A Novel Power Delivery Method for Asynchronous Loads in Energy Harvesting Systems, ACM JETC, vol. 7, no. 4, pp. 16.1-16.22 (Dec. 2011).

Robust electronics for fluctuating power supply

- Asynchronous SRAM





A. Baz, D. Shang, F. Xia and A. Yakovlev. Self-timed SRAM for Energy Harvesting Systems, Journal of Low Power Electronics, vol. 7, no. 2, April 2011, pp. 274-284, American Scientific Publishers.

Robust electronics for fluctuating power supply

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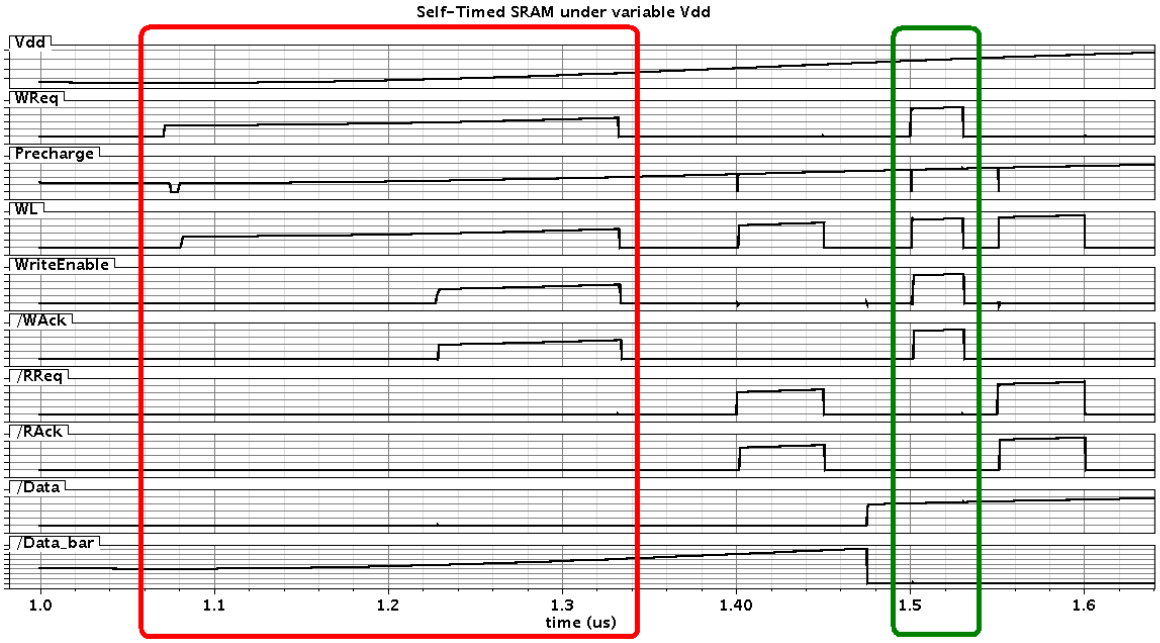
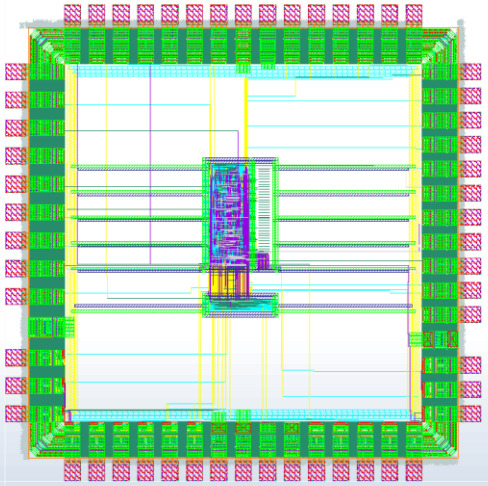


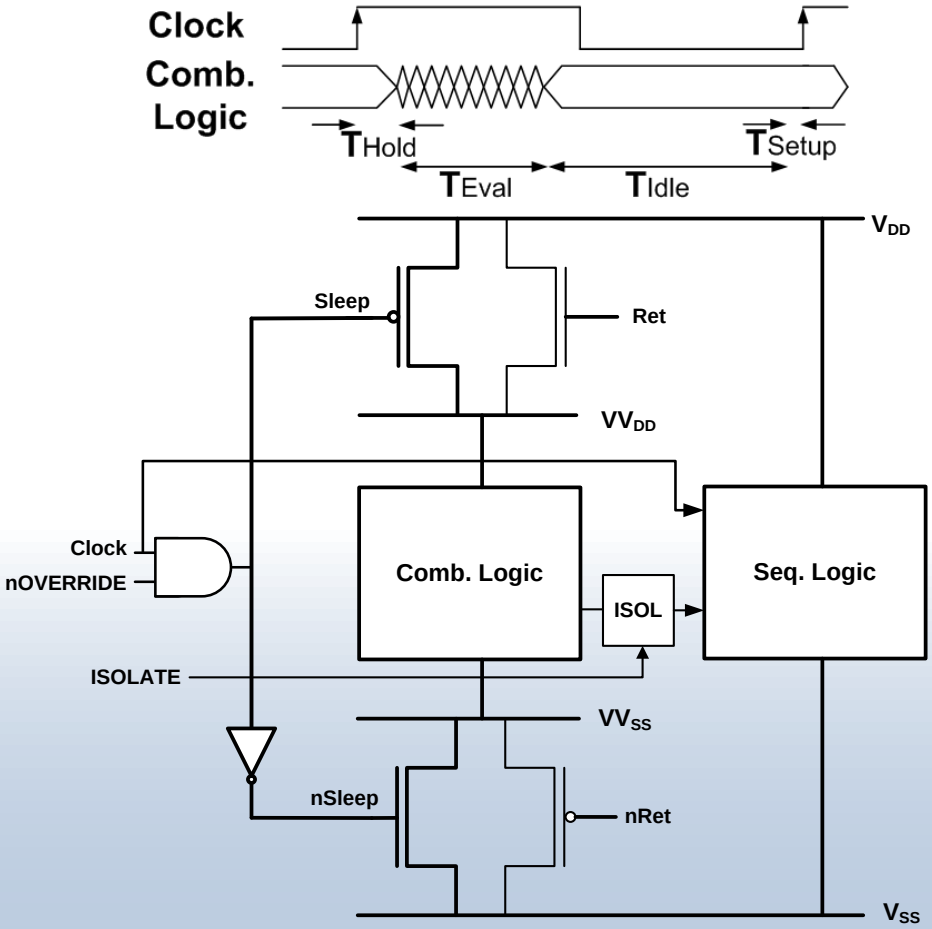
Self-timed SRAM chip:
UMC CMOS 90nm



A. Baz, D. Shang, F. Xia and A. Yakovlev. Self-timed SRAM for Energy Harvesting Systems, Journal of Low Power Electronics, vol. 7, no. 2, April 2011, pp. 274-284, American Scientific Publishers.

Active power reduction in a microcontroller through sub-clock power gating

- Aggressive frequency scaling used to achieve ultra-low power budget
  - Results in combinational idle time → leakage power
- Power gate combinational logic within clock cycle
  - Symmetric virtual rail clamping used to minimise power mode transition cost
  - Split comb. and seq logic to preserve state
  - Power gates controlled by clock



Mistry, J.N., Al-Hashimi, B.M., Flynn, D., Hill S., Sub-clock power gating technique for minimising leakage power during active, D.A.T.E. 2011, Grenoble, France, 2011.

Active power reduction in a microcontroller through sub-clock power gating

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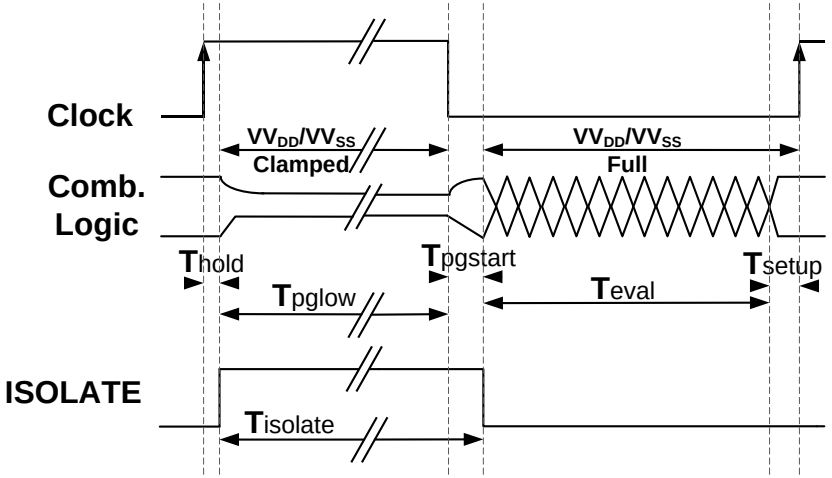
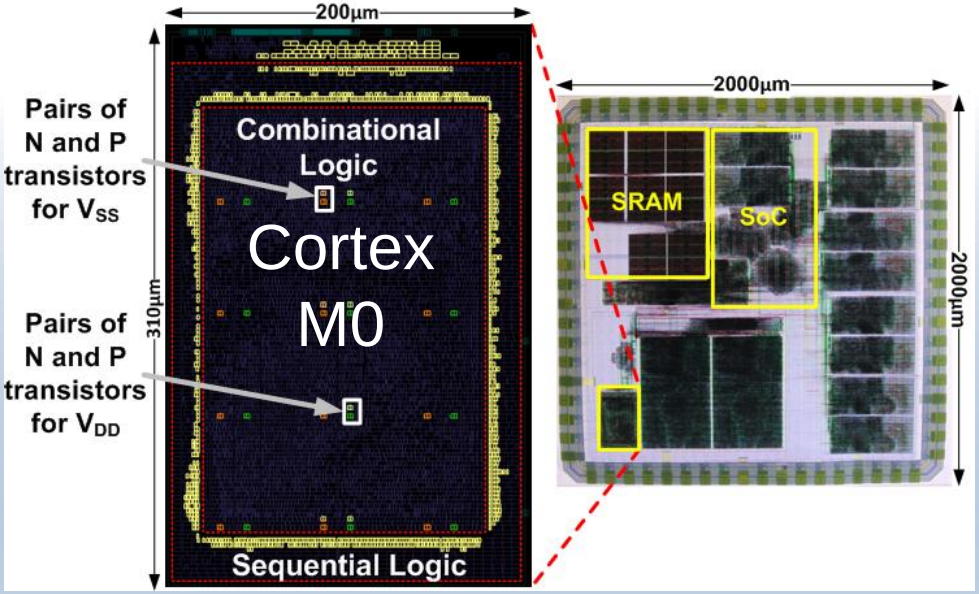
- Clock high = combinational logic 'off'
- Clock low = evaluate next state
- Output isolation used to stop short-circuit currents
- Duty cycle modulation enables highest power saving, maximise 'off' time





- Implemented on ARM Cortex-M0 microprocessor
- Fabricated on TSMC 65nm technology
- Illustrative example:

  In 12uW power budget, SCPG offers 3x improvement in energy efficiency - 100kHz (No-PG) Vs 300kHz (with SCPG)

Vision for the future

- We have a rich variety of infrastructure building blocks and through their development, new techniques at the component level
- We also have system-level designs and high-level analysis results
- An obvious next step would be to investigate the interfacing aspects, e.g. controllers and control algorithms

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Vision for the future

- On-chip sensing and monitoring in an uncertain operating environment is moving forward and is a worthy independent subject of investigation (collaboration with industry started Moortec and EPSRC grant application ONSEN pending)
- Further projects:
  - Designing systems for survival on the interface between power conditioning and computational electronics (EPSRC Responsive mode project SAVVIE awarded: Bristol&Newcastle)
  - Cross-layer (Hardware and software) energy-efficiency based on power proportionality (eFutures project PowerProp awarded)
  - Guardian Angels activity in energy autonomous sensors (EU and Programme Grant application)